**Pipelined Processor EX stage Lab**

**Robert Everhart**

**Jacob Navarro**

**Joseph Hyatt**

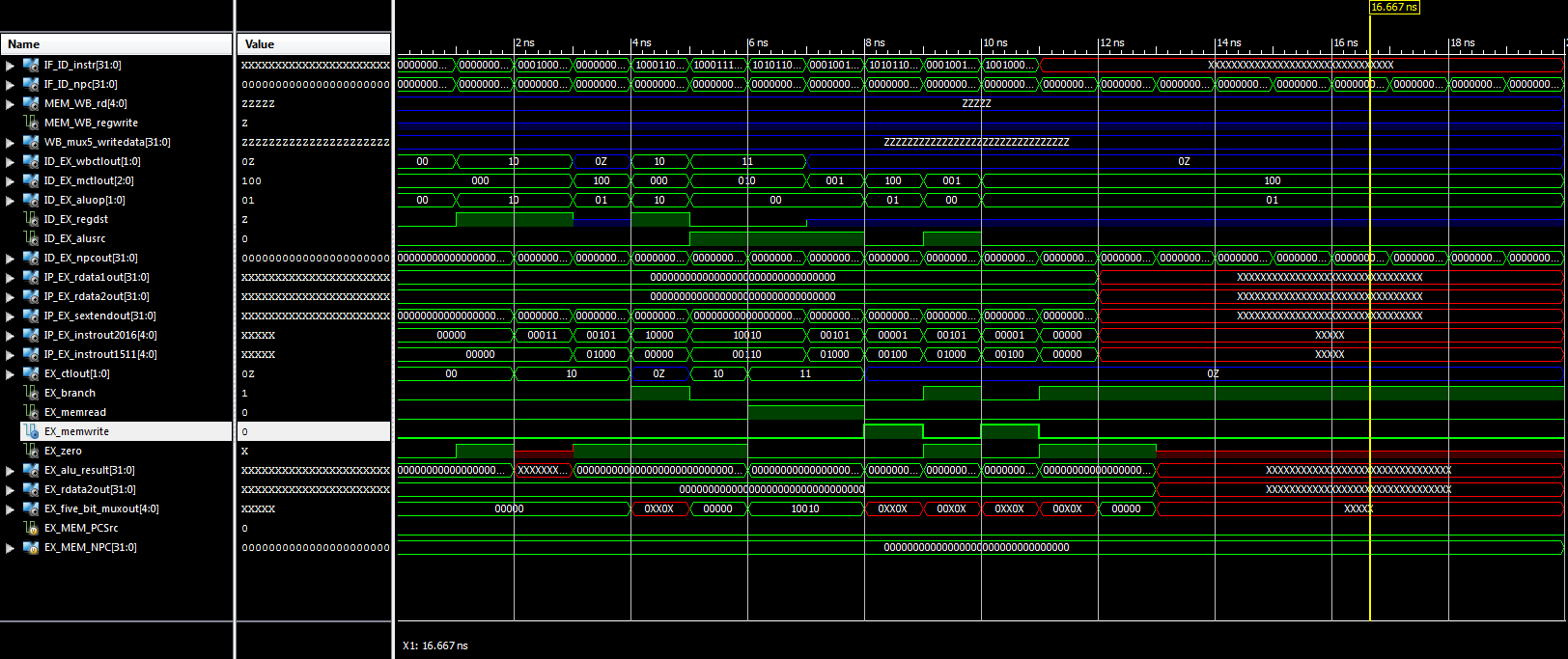
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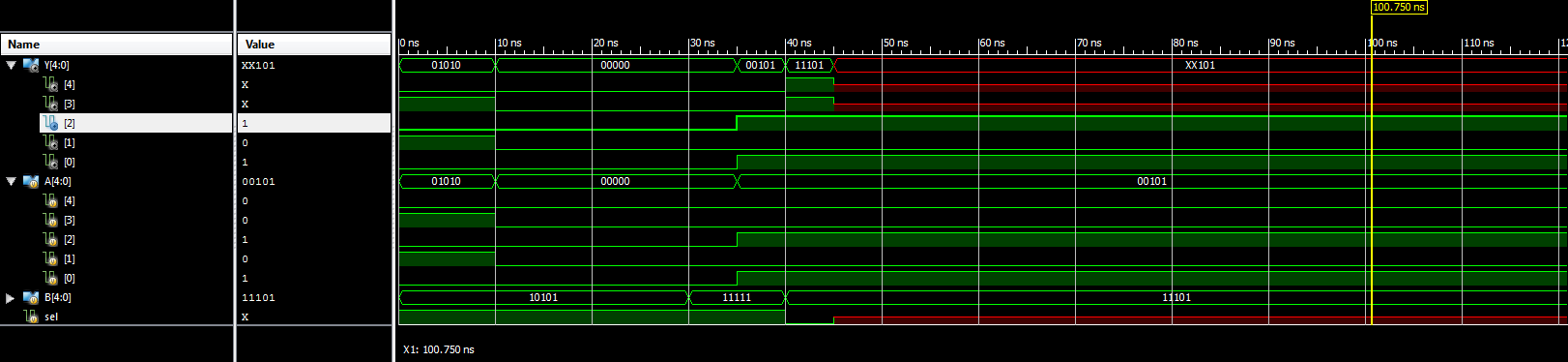
The EX (Execute stage) executes the instruction. All ALU (Arithmetic and Logic Unit) operations are done in this stage. The ALU performs operations such as addition, subtraction, shifts left and right, etc. The Execute stage will first take all the outputs from the Decode pipeline stage and make them inputs for ALU operations; this pipeline will take two register files and the register destination file. Depending on the instruction in the instruction memory, the ALU control will determine from the Decode pipeline what type of ALU operation to perform from the ALUOp 4 bit output of the control. This pipeline will also take advantage of the 5 bit RegDst from the control block to calculate the destination of the arithmetic results.

The simulations of the test benches give the following:

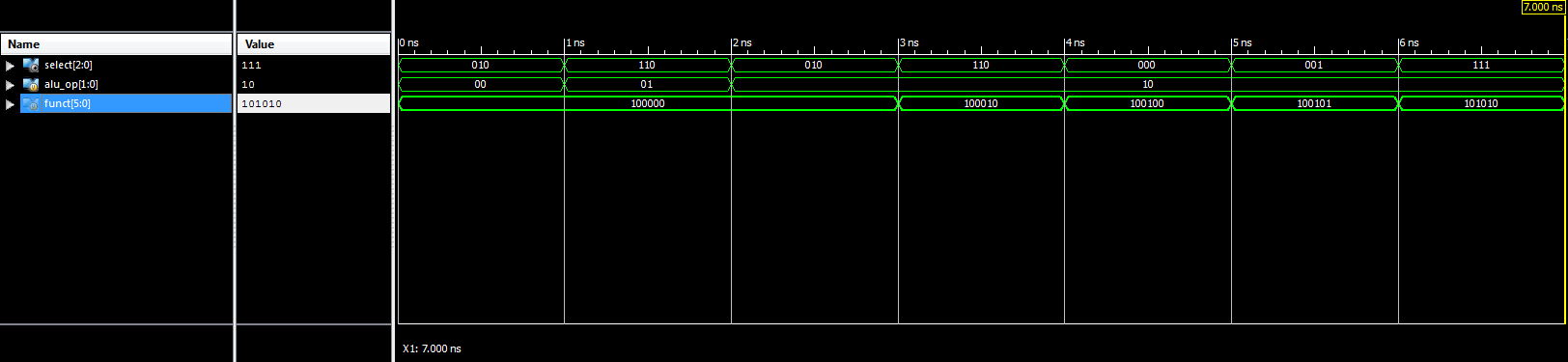
ex\_stage\_sim:



five\_bit\_mux\_tb:



alu\_control\_tb:



alu\_tb:

